

IN THE CLAIMS:

Claims 1, 5-14, 17-19, 21, 24-26, 31-36, 38, 39, 42 and 43 have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming a first dielectric layer-material upon an oxide layer-over a semiconductor substrate;

selectively removing the first dielectric layer-material to expose a plurality of areas of the oxide layer;

forming a second dielectric layer-material over the first dielectric layer-material and in contact with the plurality of exposed areas of the oxide-layer;

selectively removing the second dielectric layer-material to form a plurality of spacers at peripheral edges of the plurality of exposed areas of the oxide layer-in contact with lateral edges of the first dielectric-layer material;

removing a portion of material from the plurality of areas of the oxide layer-at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into the semiconductor substrate;

forming a liner upon a sidewall of each isolation trench of the plurality of isolation trenches;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide-layer;

depositing a conformal layer material in each isolation trench, the conformal layer-material extending over remaining portions of the oxide layer-in contact with a corresponding pair of the spacers, wherein the depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric layer-material so as to define an upper surface contour of the conformal-layer material;

removing portions of the conformal layer material overlying the remaining portions of the oxide

layer-by planarizing the conformal layer material at least to the first dielectric layer material and each spacer such that an upper surface for each isolation trench is co-planar to the other upper surfaces,

the conformal layer-material comprising a material that is electrically insulative and extends continuously between and within the plurality of isolation trenches; and removing the first dielectric layer-material and portions of the oxide layer-underlying the first dielectric layer-material such that the conformal layer-material fills each said isolation trench, and extends horizontally away from each said isolation trench upon remaining portions of the oxide-layer and sidewalls of the conformal material start on an upper surface of the semiconductor substrate and are substantially orthogonal to the upper surface contour of the conformal material.

2. (Canceled).

3. (Previously Presented) The method according to Claim 1, wherein forming a liner upon a sidewall of each isolation trench comprises thermally growing oxide on the semiconductor substrate.

4. (Previously Presented) The method according to Claim 1, wherein forming the liner upon the sidewall of the isolation trench comprises depositing a composition of matter.

5. (Currently amended) The method of claim 1, wherein implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide layer comprises forming a doped region below the termination of each of said plurality of the isolation trenches within the semiconductor substrate.

6. (Currently amended) The method according to claim 1, wherein removing portions of the conformal ~~layer-material~~ overlying the remaining portions of the oxide ~~layer~~ comprises removing portions of the conformal ~~layer-material~~ overlying the remaining portions of the oxide ~~layer~~ by chemical mechanical planarization.

7. (Currently amended) A method of forming a microelectronic structure, the method comprising:
forming a first dielectric ~~layer-material~~ upon an oxide ~~layer~~ over a semiconductor substrate;
selectively removing the first dielectric ~~layer-material~~ to expose a plurality of areas of ~~an~~the oxide ~~layer~~;
forming a second dielectric ~~layer-material~~ over the first dielectric ~~layer-material~~ and in contact with the plurality of exposed areas of the oxide ~~layer~~;
selectively removing the second dielectric ~~layer-material~~ to form a plurality of spacers at peripheral edges of the plurality of exposed areas of the oxide ~~layer~~ in contact with lateral edges of the first dielectric ~~layer-material~~;
removing a portion material from the plurality of areas of the oxide ~~layer~~ at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into the semiconductor substrate;
rounding the top edge of each of the isolation trenches;
implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide ~~layer~~;
depositing a conformal ~~layer-material~~ filling each isolation trench, the conformal ~~layer-material~~ extending over remaining portions of the oxide ~~layer~~ in contact with a corresponding pair of the spacers, wherein the depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric ~~layer-material~~ so as to define an upper surface contour of the conformal ~~layer-material~~;

removing portions of the conformal ~~layer-material~~ that overlie the remaining portions of the oxide ~~layer~~ by planarizing the conformal ~~layer-material~~ to form an upper surface for each isolation trench that is co-planar to the other upper surfaces; and
removing the first dielectric ~~layer-material~~ and portions of the oxide ~~layer~~ underlying the first dielectric ~~layer-material~~ such that the conformal ~~layer-material~~ fills each isolation trench, ~~and extends horizontally away from each isolation trench upon remaining portions of the oxide-layer and sidewalls of the conformal material begin on an upper surface of the semiconductor substrate and are oriented substantially orthogonal to the upper surface contour of the conformal material;~~

wherein:

the conformal ~~layer-material~~ comprises ~~a-material that is electrically insulative and extends continuously between and within the plurality of isolation trenches;~~
the conformal ~~layer-material~~ and the spacers form the upper surface for each isolation trench, each upper surface being formed from the conformal ~~layer-material~~ and the spacer and being situated above the oxide ~~layer~~; and
the first dielectric ~~layer-material~~ is in contact with at least a pair of the spacers and the oxide ~~layer~~.

8. (Currently amended) The method according to Claim 7, further comprising:
forming a gate oxide ~~layer~~ upon the semiconductor substrate.

9. (Currently amended) The method according to claim 7, wherein removing portions of the conformal ~~layer-material~~ comprises etching the material using an etch recipe that etches the conformal ~~layer-material~~ faster than the first dielectric ~~layer-material~~ by a ratio in a range from about 1:1 to about 2:1.

10. (Currently amended) The method according to Claim 9, wherein etching the material using an etch recipe that etches the conformal ~~layer-material~~ faster than the first dielectric ~~layer-material~~ by a ratio in a range from about 1:1 to about 2:1 comprises etching the

conformal ~~layer-material~~ the ratio is in a range from about 1.3:1 to about 1.7:1.

11. (Currently amended) The method according to claim 7, wherein removing portions of the conformal ~~layer-material~~ overlying the remaining portions of the oxide layer comprises:
chemical mechanical planarization, wherein the conformal ~~layer-material~~, the spacers, and the first dielectric ~~layer-material~~ form a planar first upper surface; and
etching to form a second upper surface situated above the ~~oxide-layer~~.

12. (Currently amended) The method according to Claim 11, wherein ~~etching to form a second upper surface removing portions of the conformal material that overlie the remaining portions of the oxide further~~ comprises etching using an etch recipe that etches the conformal ~~layer-material~~ faster than the first dielectric ~~layer-material~~ by a ratio in a range of from about 1:1 to about 2:1.

13. (Currently amended) The method according to Claim 12, wherein etching using an etch recipe that etches the conformal ~~layer-material~~ faster than the first dielectric ~~layer-material~~ by a ratio in a range from about 1:1 to about 2:1 comprises etching using an etch recipe that etches the conformal ~~layer-material~~ faster than the first dielectric ~~layer-material~~ by a ratio in a range of from about 1.3:1 to about 1.7:1.

14. (Currently amended) A method of forming a microelectronic structure, the method comprising:
forming an oxide layer upon a semiconductor substrate;
forming a silicon nitride layer upon the oxide layer;
selectively removing the silicon nitride layer to expose a plurality of areas of the oxide layer;
forming a first silicon dioxide ~~layer-material~~ over the silicon nitride layer and in contact with the plurality of exposed areas of the oxide layer;

selectively removing the first silicon dioxide ~~layer-material~~ to form a plurality of spacers at the peripheral edges of the plurality of exposed areas of the oxide ~~layer~~-in contact with lateral edges of the silicon nitride ~~layer~~;

removing a portion material from the plurality of areas at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches into the semiconductor substrate;

forming a corresponding electrically active region below the termination of each isolation trench within the semiconductor substrate;

forming a liner upon a sidewall of each isolation trench;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide ~~layer~~;

depositing a conformal second silicon dioxide ~~layer-material~~ filling each isolation trench, the conformal second silicon dioxide ~~layer-material~~ within each isolation trench and extending over remaining portions of the oxide ~~layer~~-in contact with the corresponding pair of the spacers, the depositing is carried out to the extent of filling each isolation trench and extending over the spacers and the silicon nitride ~~layer~~-so as to define an upper surface contour of the conformal second silicon dioxide ~~layer-material~~;

removing portions of the conformal second silicon dioxide ~~layer-material~~ by planarizing the conformal second silicon dioxide ~~layer-material~~ and the spacers to form an upper surface for each isolation trench that is co-planar to the other upper surfaces, wherein an electrically insulative material extends continuously between and within the plurality of isolation trenches; and

removing the silicon nitride ~~layer~~-and portions of the oxide ~~layer~~-underlying the silicon nitride ~~layer~~-such that the conformal second silicon dioxide ~~layer-material~~ fills each isolation trench, ~~and~~-extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~-and sidewalls of the second silicon dioxide material start on an upper surface of the semiconductor substrate and lie substantially orthogonal to the upper surface contour of the second silicon dioxide material.

15. (Previously Presented) The method according to Claim 14, wherein forming a liner upon a sidewall of each isolation trench comprises forming a thermally grown oxide upon a sidewall of the semiconductor substrate.

16. (Previously Presented) The method according to Claim 14, wherein forming a liner upon a sidewall of each isolation trench comprises forming a liner composed of silicon nitride.

17. (Currently amended) The method according to Claim 15, further comprising:
forming a gate oxide ~~layer-upon~~ the semiconductor substrate.

18. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide ~~layer-upon~~ a semiconductor substrate;

forming a polysilicon ~~layer-upon~~ the oxide-layer;

forming a first dielectric ~~layer-material~~ upon the polysilicon-layer;

selectively removing the first dielectric ~~layer-material~~ and the polysilicon ~~layer~~ to expose a plurality of areas of the oxide-layer;

forming a second dielectric ~~layer-material~~ conformally over the polysilicon-layer, the first dielectric ~~layer-material~~ and in contact with the plurality of exposed areas of the oxide layer;

selectively removing the second dielectric ~~layer-material~~ to form a plurality of spacers at the peripheral edges of the plurality of exposed areas of the oxide layer—in contact with lateral edges of the first dielectric-layer ~~material~~;

removing a portion of material from the plurality of areas of the oxide ~~layer~~ at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate;

rounding the top edges of each of the isolation trenches;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a

plane of the oxide-layer;
depositing a conformal third ~~layer~~ material filling each isolation trench, the conformal third ~~layer~~ material extending over remaining portions of the oxide ~~layer~~ in contact with a corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric ~~layer~~ material so as to define an upper surface contour of the conformal third ~~layer~~ material;
removing portions of the conformal third ~~layer~~ material by planarizing the conformal third ~~layer~~ material to form an upper surface for each isolation trench that is co-planar to the other upper surfaces; and
removing the first dielectric ~~layer~~ material, polysilicon ~~layer~~ and portions of the oxide ~~layer~~ underlying the first dielectric ~~layer~~ material such that the conformal third ~~layer~~ material fills each isolation trench, and extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the conformal third material extend from an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are substantially orthogonal to the upper surface contour of the conformal third material;
wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third ~~layer~~ material, and the plurality of isolation trenches.

19. (Currently amended) The method according to Claim 18, wherein removing portions of the conformal third ~~layer~~ material comprises removing portions of the conformal third ~~layer~~ material by chemical mechanical planarization.

20. (Previously Presented) The method according to Claim 18, wherein implanting comprises forming a doped region below the termination of each isolation trench within the semiconductor substrate.

21. (Currently amended) The method according to Claim 18, wherein rounding the top edges of each of the isolation trenches comprises forming a liner upon a sidewall of each isolation trench, the liner being confined preferentially within each isolation trench and extending from an interface thereof with the oxide layer to the termination of the isolation trench within the semiconductor substrate, and wherein the conformal third layer-material is composed of an electrically insulative material.

22. (Previously Presented) The method according to Claim 21, wherein forming a liner upon a sidewall of each isolation trench comprises forming a thermally grown oxide upon a sidewall the semiconductor substrate.

23. (Canceled).

24. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon the oxide layer;

forming a first dielectric layer-material upon the polysilicon layer;

selectively removing the first dielectric layer-material and the polysilicon layer to expose a plurality of areas of the oxide layer;

forming a second dielectric layer-material over the polysilicon layer, the first dielectric layer-material and in contact with the plurality of exposed areas of the oxide layer;

selectively removing the second dielectric layer-material to form a plurality of spacers at the peripheral edges of the plurality of exposed areas of the oxide layer in contact with lateral edges of the first dielectric layer-material;

removing a portion of material from the plurality of exposed areas of the oxide layer at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a

plane of the oxide-layer;
 depositing a conformal third layer material filling each isolation trench, the conformal third layer material extending over remaining portions of the oxide-layer in contact with a corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric layer material so as to define an upper surface contour of the conformal third-layer material;
 removing portions of the conformal third layer material by planarizing the conformal third layer material to form an upper surface for each isolation trench of the plurality of isolation trenches that is co-planar to the other upper surfaces;
 removing the first dielectric-layer material, polysilicon layer and portions of the oxide layer underlying the first dielectric layer material such that the conformal third layer material fills each isolation trench, and extends horizontally away from each isolation trench upon remaining portions of the oxide-layer and sidewalls of the conformal third material extend from an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are oriented substantially orthogonal to the upper surface contour of the conformal third material,
 wherein the conformal third layer material is an electrically insulative material that and extends continuously between and within the plurality of isolation trenches;
 wherein the upper surface for each isolation trench of the plurality of isolation trenches is formed from the conformal third layer material, the spacers, and the first dielectric layer material; and
 wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer material, and the plurality of isolation trenches.

25. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;
 forming a first polysilicon layer material upon the oxide-layer;
 forming a first dielectric layer material upon the polysilicon-layer;

selectively removing the first dielectric ~~layer-material~~ and the first polysilicon layer-material to expose a plurality of areas of the oxide-layer;

forming a second dielectric ~~layer-material~~ over the first dielectric ~~layer-material~~ and in contact with the plurality of exposed areas of the oxide-layer;

selectively removing the second dielectric ~~layer-material~~ to form a plurality of spacers at peripheral edges of the plurality of exposed areas of the oxide layer-in contact with lateral edges of the first dielectric-layer ~~material~~;

removing a portion of material from the plurality of exposed areas of the oxide layer-at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate;

rounding the top edges of each of the isolation trenches;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide-layer;

depositing a conformal third ~~layer-material~~ filling each isolation trench, the conformal third ~~layer-material~~ extending over remaining portions of the oxide layer-in contact with a corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric ~~layer-material~~ so as to define an upper surface contour of the conformal third-layer ~~material~~;

removing portions of the conformal third ~~layer-material~~ overlying the remaining portions of the oxide layer-by planarizing the conformal third ~~layer-material~~ to form an upper surface for each isolation trench that is co-planar to the other upper surfaces;

exposing the oxide layer-upon a portion of a surface of the semiconductor substrate;

forming a gate oxide layer-upon the portion of the surface of the semiconductor substrate;

forming between the plurality of isolation trenches, and confined in the space therebetween, a ~~layer-composed-of-second~~ polysilicon ~~material~~ upon the oxide layer-in contact with a pair of the spacers;

selectively removing the third ~~material~~layer, the spacers, and the ~~layer-composed-of-second~~ polysilicon ~~material~~ to form a portion of at least one of the upper surfaces; and

removing the first dielectric-layer ~~material~~, first polysilicon material layer-and portions of the

oxide layer-underlying the first dielectric layer-material such that the conformal third layer material fills each isolation trench, and extends horizontally away from each isolation trench upon remaining portions of the oxide-layer and sidewalls of the conformal third material originate on an upper surface of the semiconductor substrate and extend to the upper surface contour of the conformal third material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the conformal third material; wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches.

26. (Currently amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a polysilicon layer upon the oxide overlying a semiconductor substrate layer;

forming a first dielectric layer-material upon the polysilicon layer;

selectively removing the first dielectric layer-material and the polysilicon layer to expose a plurality of areas of the oxide layer;

forming a second dielectric layer-material over the polysilicon layer and the first dielectric layer material and in contact with the plurality of exposed areas of the oxide layer;

selectively removing the second dielectric layer-material to form a plurality of spacers at peripheral edges of the plurality of exposed areas of the oxide layer in contact with lateral edges of the first dielectric layer material;

removing material from the plurality of exposed areas of the oxide layer at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate;

rounding the top edges of each isolation trench of the plurality of isolation trenches;

implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide layer;

depositing a conformal third layer-material filling each isolation trench, the conformal third layer material extending over remaining portions of the oxide layer in contact with a

corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the first dielectric ~~layer~~material so as to define an upper surface contour of the conformal third ~~layer~~material;

removing portions of the conformal third ~~layer~~material overlying the remaining portions of the oxide ~~layer~~ by planarizing the conformal third ~~layer~~material to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces using an etch recipe that etches the conformal third ~~layer~~material and the spacers faster than the first dielectric ~~layer~~material by a ratio of from about 1:1 to about 2:1;

heat treating the oxide ~~layer~~, spacers and conformal third ~~layer~~material to fuse the oxide ~~layer~~, spacers and conformal third ~~layer~~material;

removing the first dielectric ~~layer~~material, polysilicon ~~layer~~ and portions of the oxide ~~layer~~ underlying the first dielectric ~~layer~~material such that the conformal third ~~layer~~material fills each isolation trench, and extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the conformal third ~~material~~ originate on an upper surface of the semiconductor substrate to the upper surface contour of the conformal third material and the sidewalls are substantially orthogonal to the upper surface contour of the conformal third ~~material~~;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third ~~layer~~material, and the plurality of isolation trenches.

27. (Previously Presented) The method according to claim 26, wherein the ratio is in a range from about 1.3:1 to about 1.7:1.

28-30 (Canceled).

31. (Currently amended) A method of forming a microelectronic structure, the method comprising:

- forming a pad oxide ~~layer~~ upon a semiconductor substrate;
- forming a first polysilicon layer-material upon the oxide-layer;
- forming a silicon nitride ~~layer~~ upon the first polysilicon-layer material;
- selectively removing the silicon nitride ~~layer~~ and the first polysilicon layer-material to expose a plurality of areas of the oxide-layer;
- forming a first silicon dioxide ~~layer-material~~ over the silicon nitride ~~layer~~ and in contact with the exposed oxide ~~layer~~ at the plurality of exposed areas of the oxide-layer;
- selectively removing the first silicon dioxide ~~layer-material~~ to form a plurality of spacers at peripheral edges of the plurality of exposed areas of the oxide ~~layer~~ in contact with lateral edges of the silicon nitride ~~layer~~ and the polysilicon-layer;
- removing a portion of material from the plurality of exposed areas at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches extending into and terminating within the semiconductor substrate, wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;
- forming a corresponding doped region below the termination of each isolation trench within the semiconductor substrate by implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide-layer;
- forming a liner upon a sidewall of each isolation trench, each liner extending from an interface thereof with the oxide ~~layer~~ to the termination of the isolation trench within the semiconductor substrate;
- rounding the top edges of the isolation trenches;

depositing a conformal second layer-material filling each isolation trench, the conformal second layer-material extending over remaining portions of the oxide layer in contact with a corresponding pair of the spacers, wherein depositing is carried out to the extent of filling each isolation trench and extending over the spacers and over the silicon nitride layer so as to define an upper surface contour of the conformal second layer-material;

removing a portion of the conformal second layer-material by planarizing the conformal second layer-material and each of the spacers to form an upper surface for each isolation trench that is co-planar to the other upper surfaces and is situated above the oxide layer; and

heat treating the oxide layer, liner, spacers and conformal second layer-material to fuse the oxide layer, liner, spacers and conformal second layer-material;

removing the silicon nitride layer, first polysilicon layer-material and portions of the oxide layer underlying the silicon nitride layer such that the conformal second layer-material fills each isolation trench, ~~and~~ extends horizontally away from each isolation trench upon remaining portions of the oxide layer and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and continue to the upper surface contour of the conformal second material, the sidewalls lie substantially orthogonal to the upper surface contour of the conformal second material;

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches.

32. (Currently amended) The method according to Claim 31, wherein each liner is a thermally grown oxide of the semiconductor substrate, and wherein the conformal second layer-material is ~~composed of an electrically insulative material~~.

33. (Currently amended) The method according to Claim 31, wherein each liner is composed of silicon nitride, and wherein the conformal second layer-material is ~~composed of an electrically insulative material~~.

34. (Currently amended) The method according to Claim 31, further comprising:
forming a gate oxide layer upon a portion of the surface of the semiconductor substrate;
forming between the plurality of isolation trenches, and confined in the space therebetween, a
layer composed of second polysilicon material upon the gate oxide layer in contact with a
pair of the spacers, and
selectively removing the layer composed of the second polysilicon material to form a portion of
at least one of the upper surfaces.

35. (Currently amended) A method for forming a microelectronic structure, the
method comprising:
forming a polysilicon layer upon an oxide layer overlying a semiconductor substrate;
forming a first layer material upon the polysilicon layer;
selectively removing the first layer material and the polysilicon layer to expose a plurality of
areas of the oxide layer;
forming a plurality of isolation trenches through the exposed oxide layer at the plurality of areas;
implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a
plane of the oxide layer;
wherein an electrically insulative material extends continuously between and within the plurality
of isolation trenches, each isolation trench:
having a spacer composed of a dielectric material upon the oxide layer in contact with the
first layer material and the polysilicon layer;
extending from an opening thereto at the top surface of the semiconductor substrate and
below the oxide layer into and terminating within the semiconductor substrate
adjacent to and below the spacer;
having a second layer material filling the isolation trench and extending above the oxide
layer in contact with the spacer, wherein filling is performed by depositing the
second layer material, and depositing is carried out to the extent of filling each
isolation trench and extending over the spacer and over the first layer material so
as to define an upper surface contour of the second layer material; and

having a planar upper surface formed from the second ~~layer~~material and the spacer and being situated above the oxide ~~layer~~, wherein the planar upper surface is formed by substantially simultaneously subjecting the entire upper surface contour of the second ~~layer~~material to a planarizing process; and removing the first ~~layer~~material, polysilicon ~~layer~~ and portions of the oxide ~~layer~~ underlying the first ~~layer~~material such that the second ~~layer~~material fills each isolation trench, and extends horizontally away from each isolation trench upon remaining portions of the oxide ~~layer~~ and sidewalls of the second ~~material~~ initiate on an upper surface of the semiconductor substrate and end at the upper surface contour of the second ~~material~~. the sidewalls are substantially orthogonal to the upper surface contour of the second material; wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second ~~layer~~material, and the plurality of isolation trenches.

36. (Currently amended) The method according to claim 35, doping the semiconductor substrate with a dopant having a first conductivity type; and wherein implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide ~~layer~~ further comprises: doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one isolation trench of the plurality of isolation trenches.

37. (Previously Presented) The method according to claim 36, wherein the doped trench bottom has a width, each isolation trench has a width, and the width of each doped trench bottom is greater than the width of the respective isolation trench.

38. (Currently amended) A method for forming a microelectronic structure, the method comprising: forming a first ~~layer~~material upon an oxide ~~layer~~ overlying a semiconductor substrate;

selectively removing the first ~~layer-material~~ to expose a plurality of areas of the oxide-layer;
forming a plurality of isolation trenches through the oxide layer-at the plurality of areas, wherein
an electrically insulative material extends continuously between and within the plurality
of isolation trenches without filling the plurality of isolation trenches, each isolation
trench:
having a spacer composed of a dielectric material upon the oxide layer-in contact with the
first-layer material;
extending from an opening thereto at the top surface of the semiconductor substrate and
below the oxide layer-into and terminating within the semiconductor substrate
adjacent to and below the spacer;
having a second ~~layer-material~~ filling the isolation trench and extending above the oxide
layer-in contact with the spacer, wherein the filling is performed by depositing the
second-layer material, and the depositing is carried out to the extent of filling each
isolation trench and extending over the spacer and over the first ~~layer-material~~ so
as to define an upper surface contour of the second-layer material; and
having a planar upper surface formed from the second ~~layer-material~~ and the spacer and
being situated above the oxide-layer, wherein the planar upper surface is formed
by removing portions of the second ~~layer-material~~ by planarizing the entire upper
surface contour of the second-layer material;
implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a
plane of the oxide-layer; and
removing the first ~~layer-material~~ and portions of the oxide-layer-underlying the first layer
material such that the second ~~layer-material~~ fills each isolation trench, and extends
horizontally away from each isolation trench upon remaining portions of the oxide-layer
and sidewalls of the second material commence at an upper surface of the semiconductor
substrate and end at the upper surface contour of the second material and the sidewalls are
oriented substantially orthogonal to the upper surface contour of the second material;
wherein the microelectronic structure is defined at least in part by the plurality of spacers, the
second-layer material, and the plurality of isolation trenches.

39. (Currently amended) The method according to claim 38, further comprising:
doping the semiconductor substrate with a dopant having a first conductivity type;
and wherein implanting ions in the plurality of isolation trenches in a direction substantially
orthogonal to a plane of the oxide ~~layer~~ further comprises;
doping the semiconductor substrate below each isolation trench with a dopant having a
second conductivity type opposite the first conductivity type to form a doped trench
bottom that is below and in contact with a respective one of the isolation trenches.

40. (Previously Presented) The method of claim 39, wherein:
the doped trench bottom has a width;
each isolation trench has a width; and
the width of each doped trench bottom is greater than the width of the respective isolation trench.

41. (Canceled).

42. (Currently amended) A method for forming a microelectronic structure, the
method comprising:
forming a polysilicon ~~layer~~ upon an oxide ~~layer~~ overlying a semiconductor substrate;
forming a first ~~layer-material~~ upon the polysilicon ~~layer~~;
forming a first isolation structure including:
a first spacer composed of a dielectric material upon the oxide ~~layer~~ in contact with the
first ~~layer-material~~ and the polysilicon ~~layer~~;
a first isolation trench extending into and terminating within the semiconductor substrate
adjacent to and below the first spacer, wherein the first spacer is situated on a side
of the first isolation trench, and wherein the first isolation trench has a top edge
that is rounded; and
a second spacer composed of a dielectric material upon the oxide ~~layer~~ in contact with the
first ~~layer-material~~ and the polysilicon ~~layer~~, the second spacer being situated on a

side of the first isolation trench opposite the side of the first spacer;
forming a second isolation structure including:

- a first spacer composed of a dielectric material upon the oxide ~~layer~~-in contact with the first ~~layer-material~~ and the polysilicon ~~layer~~;
- a first isolation trench extending into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench, and wherein the first isolation trench in the second isolation structure has a top edge that is curved; and
- a second spacer composed of a dielectric material upon the oxide ~~layer~~-in contact with the first ~~layer-material~~ and the polysilicon ~~layer~~, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

rounding the top edges of the isolation trenches;
doping the first isolation trench and second isolation trench by implanting ions in a direction substantially orthogonal to a plane of the oxide ~~layer~~;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

depositing a conformal second ~~layer-material~~ comprising an electrically insulative material, the conformal second ~~layer-material~~ filling the first and second isolation trenches and extending continuously over remaining portions of the oxide ~~layer~~-in contact with the first and second spacers of the respective first and second isolation structures, depositing is carried out to the extent of filling each of the isolation trenches and extending over the spacers and over the first ~~layer-material~~ so as to define an upper surface contour of the conformal second ~~layer-material~~;

planarizing portions of the upper surface contour of the conformal second ~~layer-material~~;

forming a planar upper surface from the conformal second ~~layer-material~~ and the first and second spacers of the respective first and second isolation structures, and being situated above the oxide ~~layer~~;

heat treating the oxide-layer, first spacer, second spacer and conformal second layer-material of the first isolation structure to fuse the oxide-layer, first spacer, second spacer and conformal second layer-material of the first isolation structure;

heat treating the oxide-layer, first spacer, second spacer and conformal second layer-material of the second isolation structure to fuse the oxide-layer, first spacer, second spacer and conformal second layer-material of the second isolation structure, and

removing the first-layer material, polysilicon layer and portions of the oxide layer underlying the first layer-material such that the conformal second layer-material fills each isolation trench, and extends horizontally away from each isolation trench upon remaining portions of the oxide-layer and sidewalls of the second material initiate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the second material;

wherein the microelectronic structure is defined at least in part by the active area, the second layer material, and the first and second isolation trenches.

43. (Currently amended) A method for forming a microelectronic structure, the method comprising:

forming a first layer-material upon an oxide layer overlying a semiconductor substrate;

forming a first isolation structure including:

- a first spacer composed of a dielectric material upon the oxide layer in contact with the first-layer material;
- a first isolation trench extending into and terminating within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge that is rounded; and
- a second spacer composed of a dielectric material upon the oxide layer in contact with the first-layer material, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

- a first spacer composed of a dielectric material upon the oxide ~~layer~~-in contact with the first-layer material;

- a first isolation trench extending into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench, and wherein the first isolation trench in the second isolation structure has a top edge that is rounded; and

- a second spacer composed of a dielectric material upon the oxide ~~layer~~-in contact with the first-layer material, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

doping the first isolation trench and second isolation trench by implanting ions in a direction substantially orthogonal to a plane of the oxide ~~layer~~;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

depositing a conformal second ~~layer-material~~ comprising an electrically insulative material to fill the first and second isolation trenches and extending continuously over remaining portions of the oxide ~~layer~~-in contact with the first and second spacers of the respective first and second isolation structures, wherein the depositing is carried out to the extent of filling each of the isolation trenches and extending over the spacers and over the first ~~layer-material~~ so as to define an upper surface contour of the conformal second ~~layer material~~;

planarizing the conformal second ~~layer-material~~ and the first and second spacers of the respective first and second isolation structures to form a planar upper surface;

heat treating the oxide ~~layer~~, first spacer, second spacer and conformal second ~~layer-material~~ of the first isolation structure to fuse the oxide ~~layer~~, first spacer, second spacer and conformal second ~~layer-material~~ of the first isolation structure;

heat treating the oxide ~~layer~~, first spacer, second spacer and conformal second ~~layer-material~~ of

the second isolation structure to fuse the oxide-layer, first spacer, second spacer and conformal second layer-material of the second isolation structure; and removing the first layer-material and portions of the oxide layer-underlying the first layer-material such that the conformal second layer-material fills each isolation trench, and extends horizontally away from each isolation trench upon remaining portions of the oxide-layer and sidewalls of the conformal second material originate on an upper surface of the semiconductor substrate and extend toward the upper surface contour of the conformal second material, the sidewalls are oriented substantially orthogonal to the upper surface contour of the conformal second material.